Quantum Dots Cellular Automata: Fault Tolerant Universal Logic Gates

Amir Fijany and Benny N. Toomarian

Jet Propulsion Laboratory,
California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109

Abstract

The main promise of Quantum Dot Cellular Automata (QCA) as a new computing paradigm is the possibility of implementing a set of universal logic gates and thus feasibility of general-purpose computing. In this paper, we analyze fault tolerance properties of the Majority and NOT Gates, as the main logic gates for implementation with QCA, in terms of fabrication defect. Our results demonstrate the poor fault tolerance properties of the conventional designs for these gates and thus the difficulty in their practical application. We propose a new approach to the design of QCA-based logic gates by considering and analyzing the behavior of two-dimensional arrays of QCA cells rather than a single cell or a few cells. We analyze fault tolerance properties of such Block Majority and NOT Gates in terms of inputs misalignment and irregularity and defect (missing cells) in assembly of the array. Our results clearly demonstrate the superior fault tolerance properties of these block gates and thus their greater potential for a practical realization. The Block Majority and NOT Gates represent a set of fault tolerant universal QCA Gates which provide the necessary building blocks for designing fully QCA-based, fault tolerant, circuits and computing architectures.

Key Words: Quantum Dots based Computing, Quantum Dots Cellular Automata, Quantum Dots Logic Gates, Universal Logic Gates, Fault Tolerant Logic Gates.

1. Introduction

Quantum dot-based computing, in general, and Quantum-dot Cellular Automata (QCA), in particular, have recently been investigated as a promising new technology capable of offering significant improvement over conventional VLSI in terms of integration level, power consumption, and switching speed [1-9]. In terms of feature size, it is expected that QCA cell of few nm size can be fabricated through molecular implementation [5]. The drastic reduction in power consumption results from the fact that in today's VLSI technology, the information is transferred with the use of electric currents, that is, the transfer of charge. In contrast, the QCA represents a *computation without current* paradigm [10] in which the information is propagated as polarization state through local interaction among QCA cells. In this sense, the QCA also represents a *wireless computing* paradigm wherein, through local interaction among cells, a linear array of

QCA cells can be used as a binary quantum wire [3]. In terms of raw speed, it has been shown that a switching time of as fast as 200 ps can be achieved [10].

Recent studies have also shown the feasibility of implementing logic gates and computing circuits by QCA. The design of a set of *universal logic gates* is shown in [4,6]. This indicates the feasibility of performing general-purpose computing with QCA-based hardware. The design of simple circuits has been demonstrated for full adder [4], multiplexer and arithmetic logic unit [11], and a bit-serial adder [12]. In addition, we have shown that QCA can be used in the design of massively parallel architectures enabling efficient systolic computation of FFT [13]. The superior features of QCA over current CMOS VLSI devices along with the feasibility of designing logic gates, circuits, and massively parallel architectures indicate the potential of QCA as a promising novel computing paradigm. In the sense that it would potentially allow the implementation of massively parallel computing architectures which could outperform the current CMOS VLSI counterparts in every performance aspect, i.e., integration density, power consumption, and speed, while also enabling new applications by overcoming inherent limitations of VLSI technology [13].

There are, however, several obstacles for a practical realization of QCA and exploiting full potential of this new computing paradigm. The first major obstacle is the realization of QCA hardware capable of performing in room temperature. Current semiconductor technologies that are being considered for the QCA implementation would operate only in cryogenic temperatures due to the large size of the cells. This, in turn, has motivated the investigation of molecular realization of QCA. The smaller size of molecules means that Coulomb energies are much larger so room temperature operation is possible [5]. In fact, there are indications that realization of QCA-based molecular devices capable of functioning in the current commercial regime is possible [10]. The second obstacle is the means by which input state is fixed and the output state is measured. Obviously, the issue of connecting the nano-world to the micro-world is one that is germane to all type of nano-devices. The third issue is the required precision in the assembly and tolerance to fabrication defect. In fact, it is widely believed that QCA devices and circuits will be highly sensitive to imprecision in their assembly [10]. Here again, it seems that molecular implementation provides an additional advantage by allowing the use of various self-assembly techniques. However, there are still questions as to whether molecular self-assembly techniques would give sufficient control over cells positioning [10].

In this paper, we present a novel approach for the design of fault tolerant QCA logic gates. Note that, the issue of fault tolerance has been so far analyzed from an implementation technology point of view. In contrast, we have studied the issue of fault tolerance from an architectural point of view [14,15]. Our approach is based upon the following conjecture. Assuming a certain amount of irregularity in the assembly of the QCA cells as well as missing cells, is it still possible to design circuits that perform the desired functions despite their faulty assembly? This is the direction that we have been pursuing as a technique for enabling fault tolerant QCA logic gates and circuits. In a recent paper, we have presented the design of fault tolerant Majority Gates. In this paper, we extend our approach to design of fault tolerant NOT Gates. These gates offer

remarkable robustness with respect to input and output misalignment, irregularity in cells assembly, and defective (or, missing) cells. These gates have been validated through simulation based on physical model. These fault tolerant Majority and NOT Gates represent a set of universal fault tolerant QCA logic and thus provide the necessary building blocks for designing fully QCA-based fault tolerant circuits and computing architectures. Our results also indicate that, contrary to the current belief, the QCA arrays through their collective and cellular behavior exhibit a very high degree of robustness.

This paper is organized as follows. In Section 2, we present a brief overview of the QCA technology. In Section 3, we first analyze fault tolerance properties of QCA logic gates, the Majority and NOT Gates. We then present our approach to design of new Majority and NOT Gates with fault tolerant capabilities. We will demonstrate robustness of these new logic gates in terms of imprecision in cells assembly and input and output locations as well as the presence of missing cells. Finally, some concluding remarks and discussion of future directions are presented in Section 4.

2. Brief Overview of QCA

In this section, we present a brief overview of basic functioning of the computing elements of QCA. More detailed discussions can be found in [3-9]. The basic computational element in QCA is a cell. A QCA cell consists of four quantum dots positioned at the corner of a square (Fig. 1a). The cell contains two extra mobile electrons which are allowed to tunnel between neighboring sites. Tunneling out of the cell is assumed to be completely suppressed by the potential barriers between cells. Indeed, if the barriers between cells are sufficiently high, the electron will be well localized on individual dots. The Coulomb repulsion between the electrons will force them to occupy antipodal sites in the square. For an isolated cell, there are two energetically equivalent arrangements of the extra electrons that are denoted as cell state or polarization, P. The cell polarization is used to encode binary information (Fig. 1a). The polarization of a non-isolated cell is determined based on interaction with neighboring cells. The interaction between cells is Coulombic and provides the basis for computing with QCA. No current flows between cells and no power or information is delivered to individual internal cells. Local interconnections between cells are provided by the physics of cell-cell interaction [6]. This Coulombic interaction among cells enables a linear array of QCA cells to act as a binary wire (Fig. 1b). In such a binary wire, the information is propagated as polarization state through local interaction among QCA cells. That is, if the input cell is kept in a given polarization then this polarization, as a result of Coulombic interaction, propagates through the QCA array.

Previous results have demonstrated the feasibility of fabricating quantum dots with single charge [1] and of making large arrays of dots and controlling their occupancy [2]. The design of quantum binary wire and co-planar line crossing using QCA is presented in [3,4,6]. The design of a set of universal logic gates based on the Majority Gate and the NOT Gate (Inverter Chain) is presented in [4,6] as depicted in Figs.1c and 1d. The first experimental demonstration of a functioning QCA cell is presented in [7]. Experimental

demonstrations of a functioning QCA binary wire and a Majority Gate are presented in [8, 9].

3. Fault Tolerant QCA Logic Gates

The Majority Gate (Fig. 1d) together with the NOT Gate (Fig. 1c) represent a set of *Universal Logic Gates*. The feasibility of designing a set a universal indicates, in turn, the possibility of general-purpose computing by QCA hardware. However, as shown below, the proper functioning of these proposed designs for both gates strongly depends on the precision in the implementation. In order to assess the impact of precision, we first analyze and validate various configurations for implementation of both gates by allowing certain imprecision in the implementation. Our results clearly demonstrate that proper functioning of both gates requires an accuracy of less than half a cell size in the implementation. This will be a critical limiting factor for any and particularly molecular realization of QCA hardware. In fact, for a future molecular implementation of QCA with a cell size of 2 nanometer, this indicates that a precision on the order of sub-nanometer is needed in the assembly of conventional Majority and NOT Gates!
In addition to limited robustness capabilities of these gates, that will be in the heart of any future QCA device, another difficulty in their practical implementation is patterning a circuit. That is, if such gates are used within a QCA circuit (i.e., their inputs are provided by other gates and their outputs act as inputs to another gates) then a high degree of accuracy (on the order of half a cell size) is also needed for proper alignment of their input and output cells. With today's technology (semiconductor or molecular), it is very hard to assemble a specific pattern, let alone making it precise. This issue should also be considered in the context of another problem associated with the manufacturing of a large number of cells with subatomic resolution and the control over position of every cell. It is believed that QCA architectures could eventually be implemented with self-assembled molecules, although there are no candidates as yet and there are questions to whether molecular assemblies would give enough control over cell positioning (Smith, 1999). This suggests that, while ultimately QCA arrays with a very large number of cells can be implemented, the exact positioning of cells would be hard to control. In other words, practical implementation QCA array would represent a high degree of irregularity in cell positioning.

To overcome the limited robustness of QCA gates and also the difficulty in patterning QCA circuits, we investigate the design of QCA logic gates from a totally different perspective. In fact, instead of analyzing the behavior of a single cell (as in Majority Gate) or few cells (as in NOT Gate) as the logic devices, we analyzed the collective behavior of various 2D arrays of cells to develop *block logic gates*. We analyze and validate regular, irregular, and irregular and defective QCA arrays for implementation Majority and NOT Gates.

The validations in this paper are performed through simulation by using AQUINAS (A Quantum Interconnected Network Array Simulator) that has been developed at the University of Notre Dame. This simulator encapsulates the physics of Hartree-Fock model for simulation of QCA array [6]. The various configurations presented in this

paper assume a dot diameter of 5nm and a cell size of 20 nm with an inter-cells distance of 14 nm (see Fig. 1b). Although, these configurations have been validated for all the possible combinations of the input values, here we only present one typical input case. Furthermore, due to lack of space, only few representative configurations are presented in this paper. More detailed study can be found in [14,15].

3.1 Fault Tolerant Majority Gates

The Majority Gate represents a logic gate that is *intrinsically* suitable for implementation with QCA. In fact, a CMOS implementation of the Majority Gate requires 12 transistors [16] whereas its QCA implementation requires only one cell (Fig. 1d). Furthermore, the logic OR and AND gates can simply be achieved by fixing one of the inputs of the Majority Gate to 1 and 0 binary values, respectively [6]. The basis of functioning of the Majority Gate can be easily understood by considering Coulombic interaction among four neighboring QCA cells. However, this also suggests that the correct functioning of such a gate would strongly depend on the precision and geometry of its implementation. In order to assess the impact of the precision and geometry, we have studied and validated various configurations for implementation of the Majority Gate.

A. Robustness of Conventional Design for Majority Gate

Figures 2.a and 2.b show functioning designs for Majority Gates with imprecise assembly in which input and output cells are all equally rotated around the device cell. Note that, Fig. 2b shows an assembly with 45 degrees rotation angle. Figure 2.c shows another functioning Majority Gate wherein the horizontal input cell is displaced upward by half a cell size with respect to the device cell. Obviously, due to symmetricity, the direction of the cell movement is not important. However, as shown in Fig. 3, if one or both of the vertical input cells are displaced by more than half a cell size with respect to the device cell, then the ensemble ceased to properly function as a Majority Gate.

Another parameter that we have studied is the imprecision in cells placement. As shown in Fig. 4, if one or both vertical input cell(s) is (are) misplaced by more than half a cell size (10 nm) with respect to device cell, then the design does not function as a Majority Gate. Surprisingly, however, the Majority Gate exhibits a much greater tolerance with respect to the displacement of the horizontal input cell. As shown in Fig. 5, the design can properly function as a Majority Gate even if the horizontal input cell is displaced by up to 70 nm with respect to the device cell.

Our study of fault tolerance properties of conventional design of Majority Gate clearly indicates that, despite exhibiting certain tolerance with respect to imprecision in its implementation, such a design is highly sensitive to misplacement and misalignment of its input cells. In particular, the results presented in Fig. 4 clearly demonstrate this sensitivity since they show that a very high accuracy on the order of smaller than half a cell size is required in positioning of the vertical input cells.

B. Fault Tolerant Block Majority Gates

Figure 6 shows a regular array of QCA cells which functions as a Block Majority Gate (The pink colored cells in the figures depict an input cell). Based on our simulation, the property of this Block Majority Gate is independent of the bock size. And, although we have done simulation by using different array's size to verify our results, here we are presenting only results for a bloc of 11 by 8 cells. This configuration has the following features that have been validated via simulation. First, it can tolerate displacement in inputs position. Basically, an input cell can be any of the 8 horizontal or 11 vertical cells. Second, it also exhibits tolerance with respect to input resolution, i.e., more than one cell can be used as input and they can also be misaligned as depicted in Fig. 8b.

These remarkable and interesting collective behaviors of regular QCA arrays are important from robustness point of view and they may also alleviate some of the problems related to pattering circuits. Note that, while these results demonstrate some rather interesting collective behavior of QCA arrays, they can be easily understood given the assumed regularity of the arrays. Obviously, this is an unrealistic assumption for any practical realization since, as stated before, the main manufacturing bottleneck is in the precise and thus regular assembly of a large number of QCA cells. To this end, we have analyzed the behavior of irregular arrays wherein the cells are randomly misplaced as depicted in Figure 7. Despite its irregularity, this array properly functions as a Block Majority Gate. As shown in Fig. 7b, it also exhibits tolerance with respect to misalignment of its inputs.

Another parameter that we have studied is the presence of defective cells. For the purpose of this study, a defective cell is one that does not participate in the Columbic interactions. From this point of view, the cell is being considered missing. This can happen during fabrication or its lifetime usage. In space application, for example, radiation may damage a cell.

Figure 8a shows an irregular and defective QCA array which function as a Block Majority Gate. Note that the location of the defective cells has been selected randomly. However, depending on the number, pattern, and location of defective cells, it could be expected that the array might cease to function as a Block Majority Gate. Figure 8b shows another irregular and defective QCA array that does not function as a Block Majority Gate. This clearly indicates that the logic function of a given irregular and defective array depends on the pattern of irregularity and particularly defection. However, this dependency should be considered in the context of relative location of inputs with respect to pattern of defection. In fact, as is shown in Fig. 8c, the same defective array of Fig. 8b can properly function as a Block Majority Gate if multiple cell (three cells) are used as input. This indicates that using multiple cell inputs seems to better guarantee the proper functioning of an irregular and defective array as a Majority Gate.

3.2 Fault Tolerant NOT Gates

The basis of functioning of conventional design of the NOT gate, as suggested in [4,6], can be better understood by distinguishing two functions, branching (or, copying) and merging, as shown in Fig. 1c. Proper branching or copying the polarization of a given cell into another cell, as for the case of QCA wire (Fig. 1b) requires precise alignment of the two cells. In contrast, the merging of two similar polarizations, to achieve inverse polarization, requires that the merging cell be precisely misaligned (i.e., 45 degree rotated) with respect the two cells. Clearly, the proper functioning of such a design strongly depends on the precision and geometry of implementation. In the following, we analyze the impact of precision and geometry of the assembly on the behavior designs for NOT Gate.

A. Robustness of Conventional Design for NOT Gate

Figure 9 shows imprecise but functioning designs for NOT Gate wherein the top row has been misplace by half a cell size (Fig. 9a) and by a cell size (Fig. 9b). Note that, for both cases, the input polarization, instead of being copied into top row, is inverted. Nevertheless, the ensemble still properly functions as a NOT Gate. However, as is shown in Fig. 10, if both top and bottom rows are misplaced by half a cell size or a cell size, then the ensemble ceases to properly function as a NOT Gate. Therefore, as for the case of Majority Gate, it can be concluded that proper functioning of conventional design for NOT Gate requires a precision on the order of less than half a cell size in the assembly.

It should be mentioned that, as shown in Fig. 11, much simpler designs can be considered for implementation of the NOT Gate. Figure 11a shows such a functioning design in which the bottom row is eliminated. At the extreme, a NOT Gate can be simply implemented by using only two cells, one for input and one for output. As shown in Figs 11b and 11c, such a simple design properly functions as a NOT Gate if the two cells are misaligned by at least half a cell size. Furthermore, it can be shown that such a simple design can also tolerate misplacement between the two cells. The results presented in Figs. 11b and 11c also explain the behavior of Block NOT Gate as well as fault tolerance of QCA wire, discussed below.

B. Fault Tolerant Block NOT Gates

As for the case of Block Majority Gate, we first consider the design of Block NOT Gate by using a regular QCA array as shown in Fig. 12. However, the proper functioning of this Block NOT Gate requires a very high precision in placement of the input cell in the sense that it should be misaligned by half a cell size with respect to the neighboring cells.

Figure 13 shows an irregular array that functions as Block NOT Gate. Interestingly, we have found out that it is rather hard to design Block NOT Gate by using irregular arrays. And, in fact, a high degree of irregularity (i.e., misplacement by more than half a cell size between neighboring cells, as in Fig. 13) is needed to be able to design Block NOT Gate.

Note that, this behavior can be explained based on the results in Figs. 11a and 11b. However, the presence of defect in the assembly allows an easier design of Block NOT Gates. This can be explained based on the fact that the defect represents a special case of irregularity wherein two neighboring cells are misplaced by more a cell size and thus allowing the polarization inversion to take place. Figures 14 shows two irregular and defective arrays, with random patterns of irregularity and defect, which properly function as Block NOT Gate.

Figure 15 shows another irregular and defective array Block NOT Gate which exhibits a high degree of tolerance with respect to input cell location. However, as for the Block Majority Gate, it could be expected that depending on the pattern of irregularity and particularly on the number, pattern, and location of defective cells, a given array might not function as a Block Majority Gate. Figure 16 shows an irregular and defective QCA array that does not function as a Block NOT Gate. Again, this clearly indicates that the logic function of a given irregular and defective array depends on the pattern of irregularity and particularly defection. However, as for the case of Majority Gate, this dependency should be considered in the context of relative location of input with respect to pattern of defection. In fact, as is shown in Fig. 17, the same defective array of Fig. 16 can properly function as a Block NOT Gate if multiple cell (two or three cells) are used as input. This again confirms the fact that using multiple cell inputs seems to better guarantee the proper functioning of an irregular and defective array as a NOT Gate.

4. Conclusion and Future Works

In this paper, we analyzed the fault tolerance properties of the conventional design for Majority Gate as the main logic gate for designing QCA circuits. Our study clearly demonstrates the limited fault tolerance capabilities of such a design and thus the difficulty in its practical usage. Clearly, this issue will be a stumbling block in realization of QCA-based hardware using nano scale cells. To overcome this problem, we proposed and studied a new approach to the design of QCA-based Majority Gate by considering collective behavior of arrays of QCA cells rather than a single cell. We analyzed robustness of such a Block Majority Gate in terms:

- *inaccuracy in the inputs location,*
- *Misaligned and irregularly spaced cells, and*
- *Defective (missing) cells in the array.*

Our simulation results demonstrate the superior fault tolerance capabilities of Block Majority Gates and its potential for a practical realization. We also showed the possibility of designing QCA circuits by using Block Majority Gates.

It should be emphasized that we have performed an extensive simulation of various Block Majority Gates from which only representative results have been presented in this paper. However, the results presented in this paper should be considered as a first attempt at understanding and analyzing the fault tolerance issues in the design of QCA hardware. Nevertheless, our results demonstrate the potential of the proposed new approach to the

design and analysis of QCA-based logic gates and circuits. They also motivate further studies as suggested below.

a) More simulation of various Block Majority Gates is needed to develop a comprehensive understanding of robustness potentials and capabilities of QCA-based hardware. In particular, more simulations and studies of irregular and defective blocks, with multiple cell inputs, need to be conducted.

b) The Majority Gate combined with the Inverter Chain (NOT Gate) represents a set of QCA-based universal logic gates. In order to develop a set of fault tolerant QCA-based universal logic gate, fault tolerant block NOT Gates need to be developed.

c) As stated before, we have conduct simulations by considering various array sizes. However, it seems that the ultimate choice of array's size would depend on two factors. First, an array might be designed to implement more complex logic function than a Majority Gate. Second, as shown in Fig. 12, a sub-array performing some logic function is distinguished from other sub-arrays by its specific clock. Therefore, the size of such a sub-array will also depend on the implementation technology and the possible resolution in realization of the clocking scheme.

d) In this paper, we focused on fault tolerance in terms of assembly of QCA cells and assuming that each cell can be precisely fabricated. In fact, as discussed in (Smith, 1999) the proper functioning of a single QCA strongly depends on precision in its assembly, i.e., dot diameter, intercell separation, etc.. However, in order to fully analyze the fault tolerance properties of QCA gates and circuits by also taking into account fabrication defects in cell assembly, more powerful simulation tools are needed. This is the topic of a current collaboration between JPL and University of Notre Dame.

Acknowledgment

The research described in this paper was performed at the Jet Propulsion Laboratory (JPL), California Institute of Technology, under contract with National Aeronautics and Space Administration (NASA). The Revolutionary Computing Technologies Program of the JPL's Center for Integrated Space Microsystems (CISM) supported this work. The authors gratefully acknowledge Professors C.S. Lent and P.M. Kogge from University of Notre Dame for insightful discussions as well as for providing us with AQUINAS simulation tool. Thanks are also due to K. Modarress for performing simulations.

References

[1] Ashoori, R.C., Stormer, H.L., Weiner, J.S., Pfeiffer, L.N., Baldwin, K.W., & West, W. (1993). N- electron ground state energies of a quantum dot in a magnetic field. *Phys. Rev. Lett.*, vol. 71, p. 613.

[2] Meurer, B., Heitmann, D., & Ploog, K. (1992). Single electron charging of quantum-dot atoms. *Phys. Rev. Lett.*, vol. 68, p. 1371.

[3] Lent, C.S., & Tougaw, P.D. (1993). Line of interacting quantum-dot cells: a binary wire. *J.*

Applied Physics, vol. 74, p. 6227.
[4] Tougaw, P.D., & Lent, C.S. (1994). Logical device implementation using quantum cellular automata. *J. Applied Physics*, 75, p. 1818.
[5] Lent, C.S., Tougaw, P.D., & Prod, W. (1994). Quantum cellular automata: The physics of computing with quantum dot molecules. *PhysComp 94: Proc. Workshop Phys. Comp.*, IEEE Computer Society Press.
[6] Lent, C.S., & Tougaw, P.D. (1997). A device architecture for computing with quantum dots. *Proc. IEEE*, vol. 85(4), p. 541.
[7] Amlani, I., Orlov, A.O., Bernstein, G.H., Lent, C.S., & Snider, G.L. (1997). Realization of a functional cell for quantum-dot cellular automata. *Science*, vol. 277, p. 289.
[8] Orlov, A.O., Amlani, I., Toth, G., Lent, C.S., Bernstein, G.H., & Snider, G.L. (1997). Experimental demonstration of a binary wire for quantum-dot cellular automata. *Applied Physics Lett.*, vol. 74, p. 928.
[9] Amlani, I., Orlov, A.O., Toth, G., Lent, C.S., Bernstein, G.H., & Snider, G.L. (1999). Digital logic gate using quantum-dot cellular automata. *Applied Physics Lett.*, vol. 74, p. 2875.
[10] Smith, C.G. (1999). Computation without current. *Science*, Vol. 284, p. 274.
[11] Gin, A., Williams, S., Meng, H., & Tougaw, P.D. (1999). Hierarchical design of quantum-dot cellular automata devices. *J. Applied Physics*, vol. 85, p. 3713.
[12] Fijany A., Toomarian, B.N., Modarress, K., and Spotnitz, M. (2001). Quantum dots-based hardware architecture for implementation of a bit-serial adder. To appear in *NASA J. of Tech Brief*.
[13] Fijany A., Toomarian, B.N., and Spotnitz, M. (1999). Novel highly parallel architectures using quantum dot-based hardware. *Proc. Parallel Computing 99* (PARCO 99), Delft, The Netherland.
[14] Fijany A. and Toomarian B.N., (2001). New Design for Quantum Dots Cellular Automata to Obtain Fault Tolerant Logic Gates. To appear in *J. Nano Particle Research*.
[15] Fijany, A., Toomarian, B.N., & Modarress, K. (2001). Quantum dots cellular automata fault tolerant logic gates: block gates with imprecise assembly. To appear in *NASA J. of Tech Brief*.
[16] Kogge, P. (1999). *Personal Communications*.

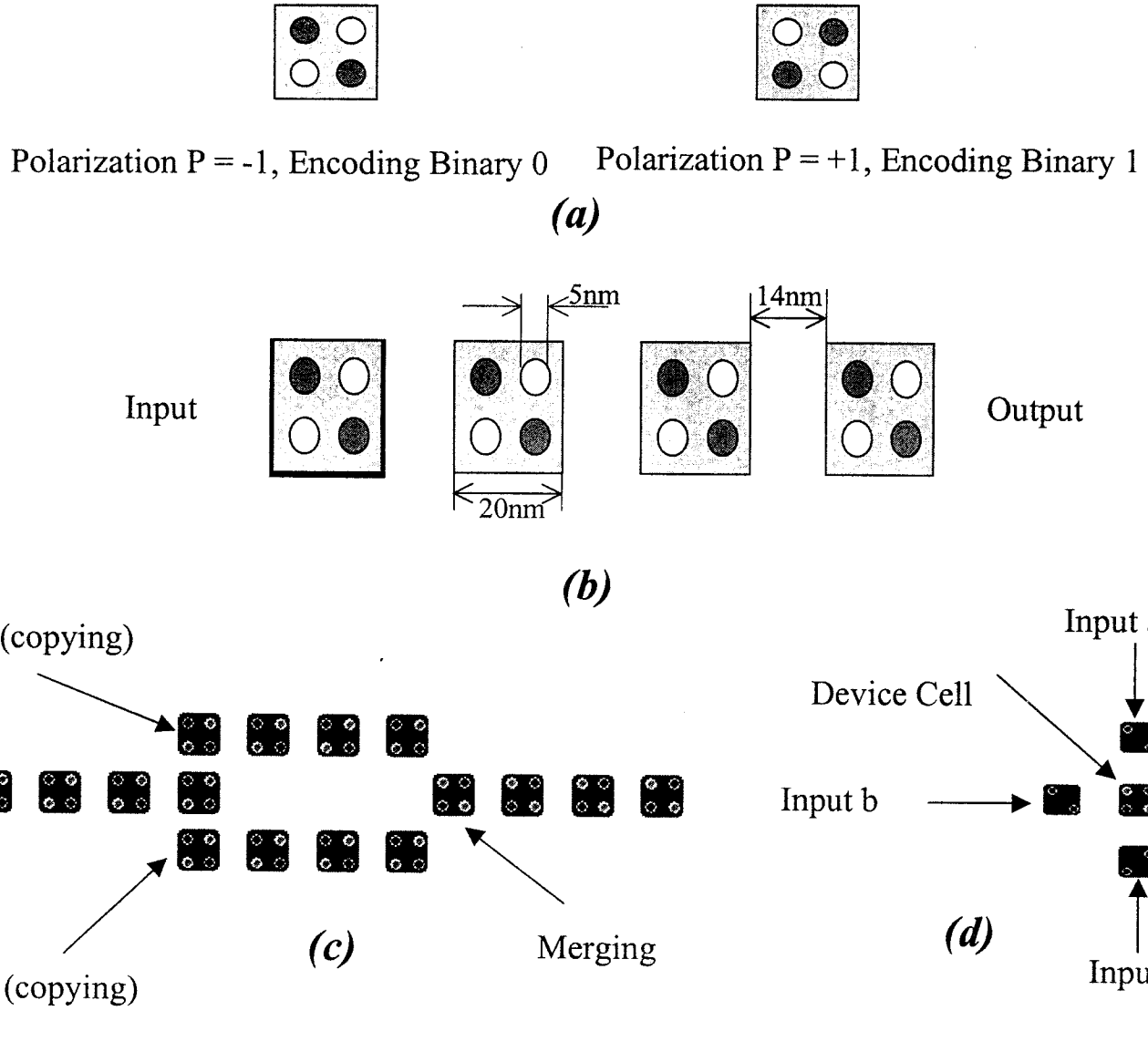

Figure 1. QCA components: (a) QCA Cell and Binary Information Representation; (b) A QCA Binary Wire; (c) Inverter Chain (NOT Gate); (d) Majority Gate

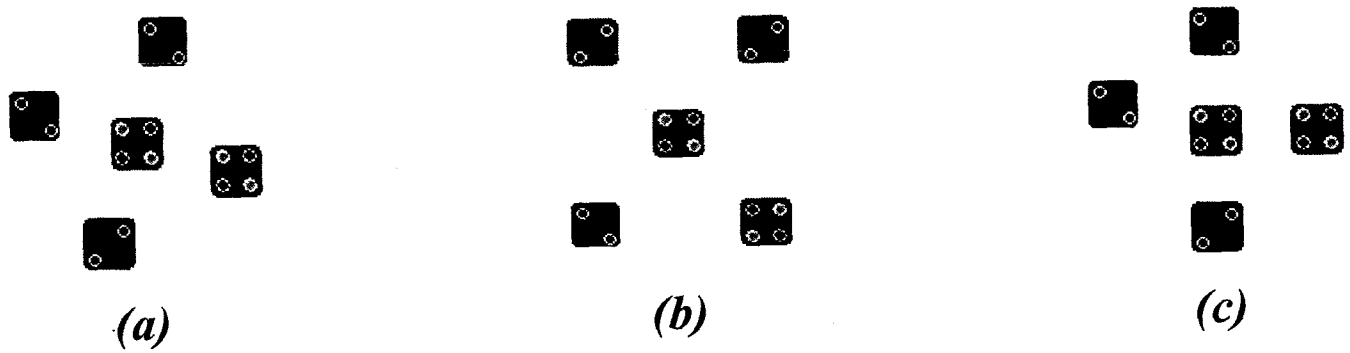

Figure 2. Functioning Majority Gates with imprecise assembly.
(a) and (b): Input and output cells are equally rotated around the device cell.
(C): Horizontal input cell is displaced by half a cell size with respect to device cell.

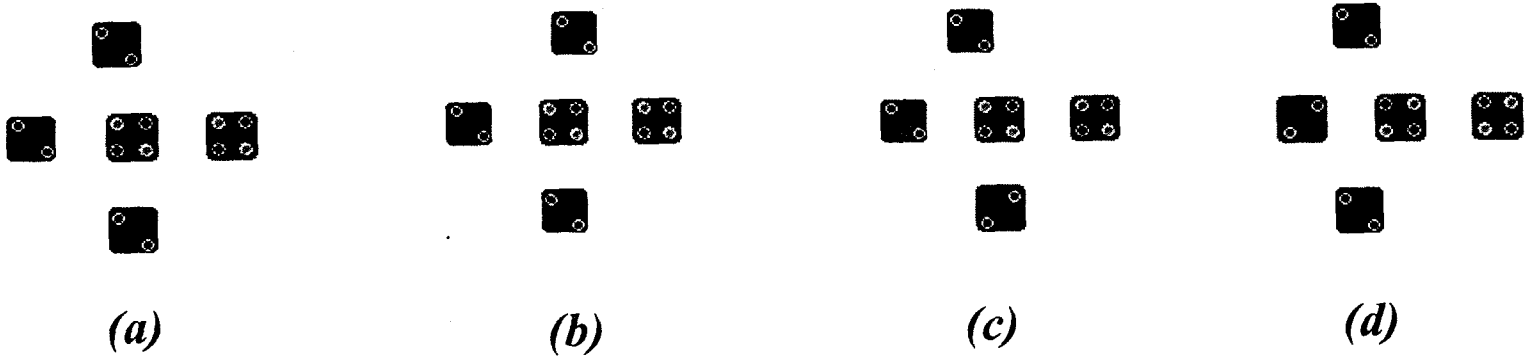

Figure 3. Imprecise assemblies for Majority Gate.
(a) and (b): Functioning designs wherein vertical input is misplaced by less than half a cell size with respect to device cell.
(c) and (d): Non-functioning designs wherein one (c) or both (d) vertical input cell(s) is (are) misplaced by more than half a cell size with respect to device cell.

Figure 4. Non-functioning designs for Majority Gate with imprecise assembly. One (a) or both (b) vertical input cell(s) is (are) displaced by half a cell size (10 nm) with respect to device cell.

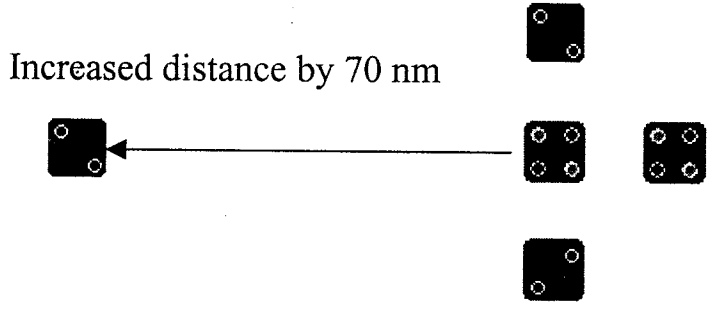

Figure 5. A functioning design for Majority Gate with imprecise assembly. The horizontal input cell can be displaced by up to 70 nm with respect to device cell.

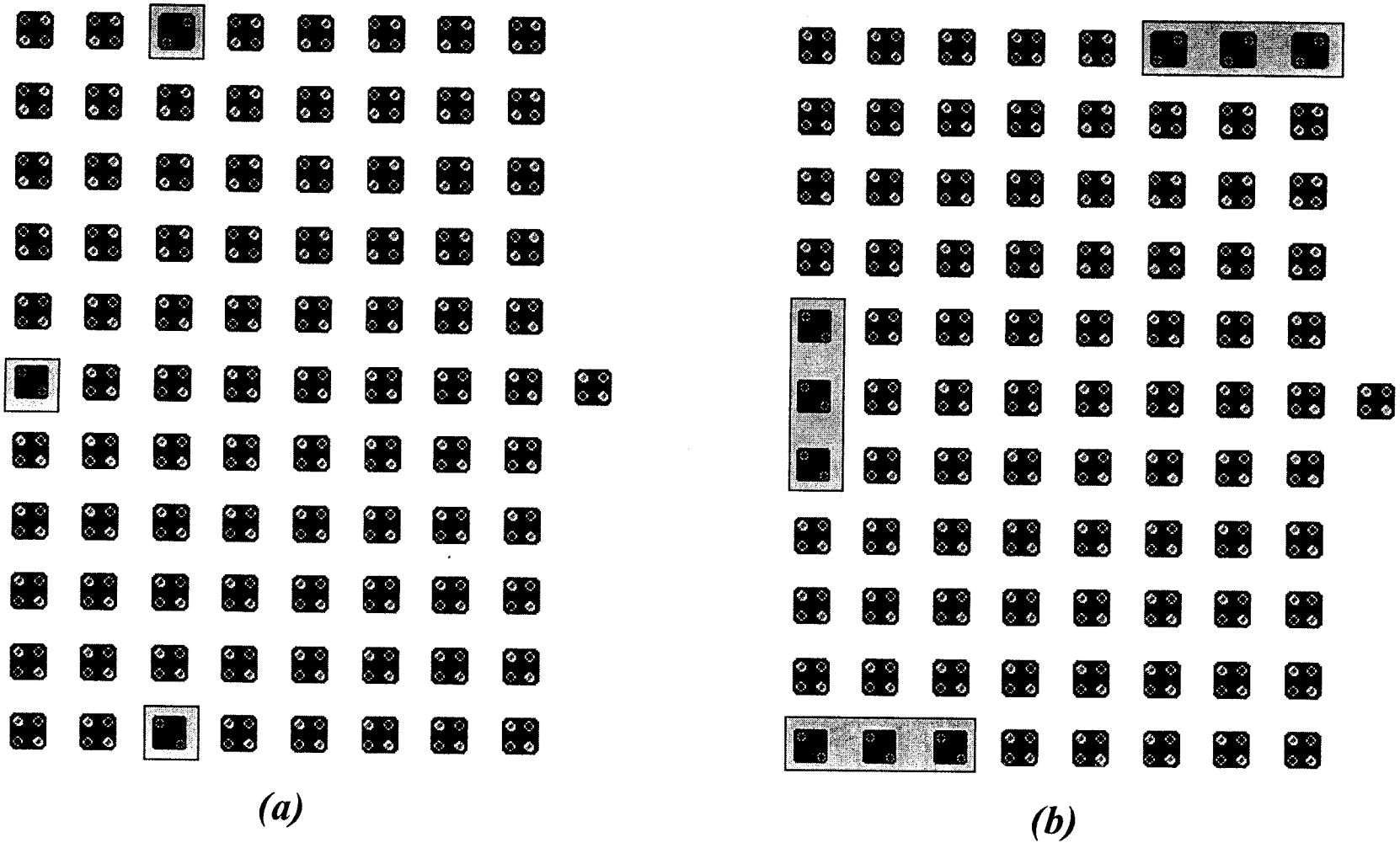

Figure 6. A QCA Block Majority Gate with precise (regular) assembly. a) Single cell input; b) Multiple cell and misaligned inputs.

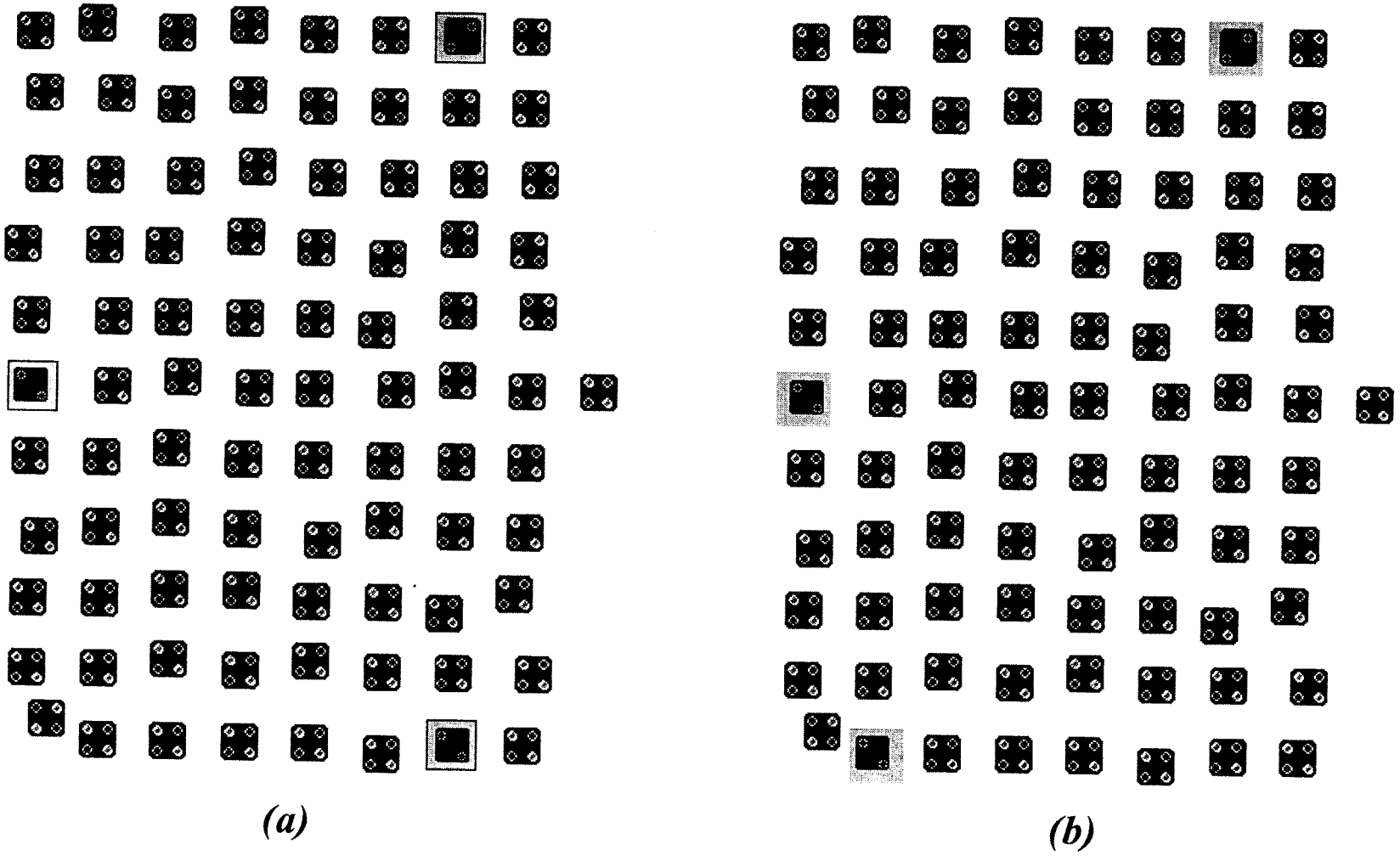

Figure 7. A QCA Block Majority Gate with irregular assembly.
a) Precisely aligned inputs; b) Misaligned inputs.

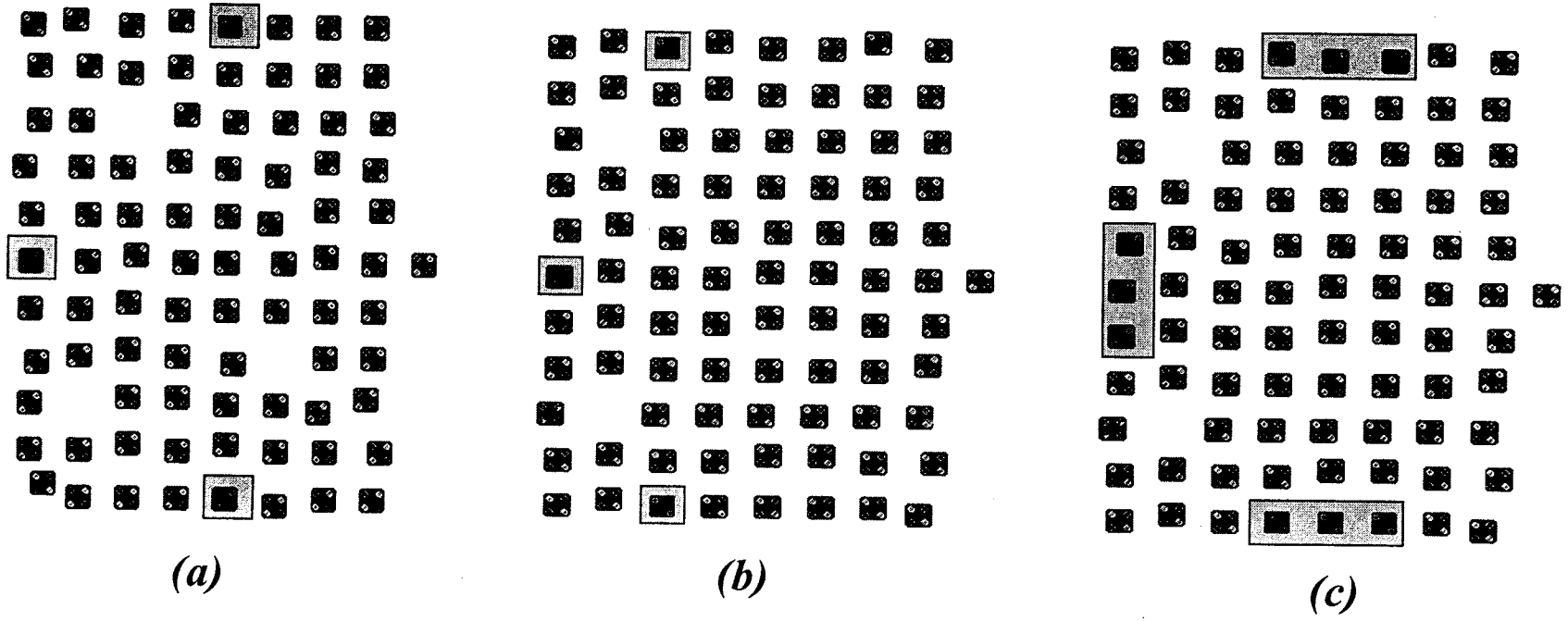

Figure 8. QCA arrays with irregular and defective (missing cells) assembly.
a) A functioning Block Majority Gate; b) A non-functioning design for Block Majority Gate;
d) A functioning Block Majority Gate using array of (b) with multiple cell inputs.

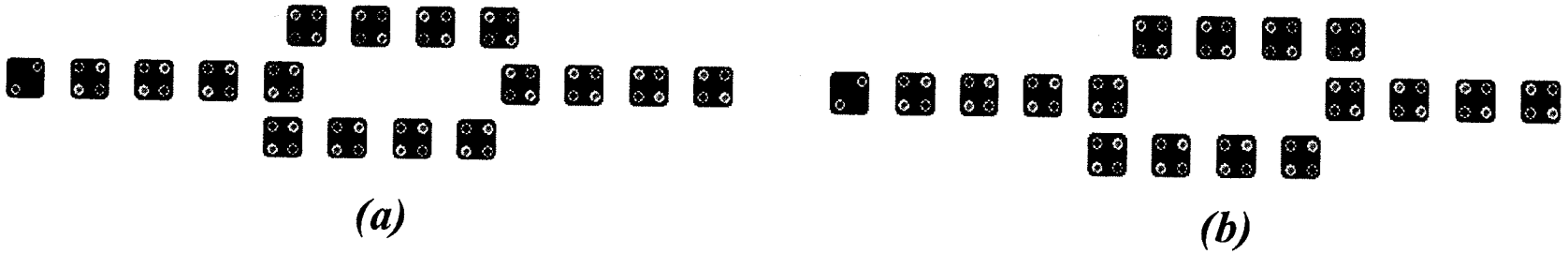

Figure 9. Functioning designs for NOT Gate

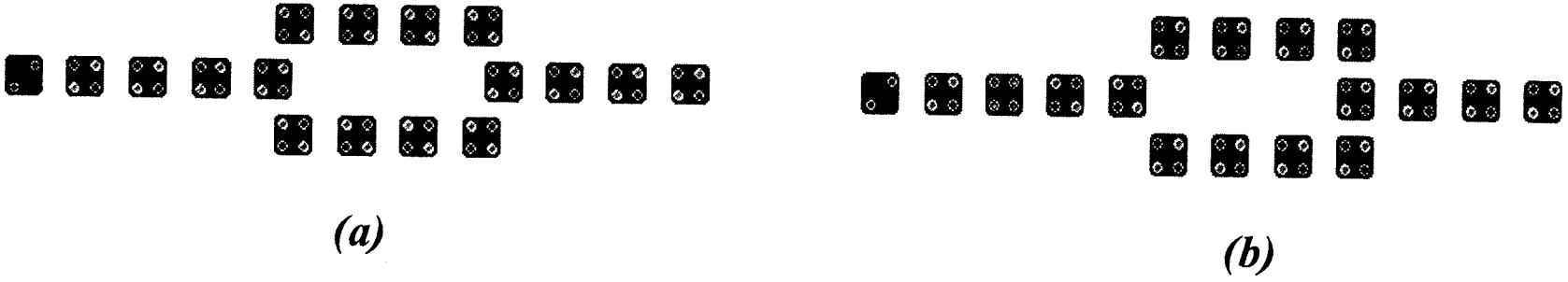

Figure 10. Non-functioning designs for NOT Gate

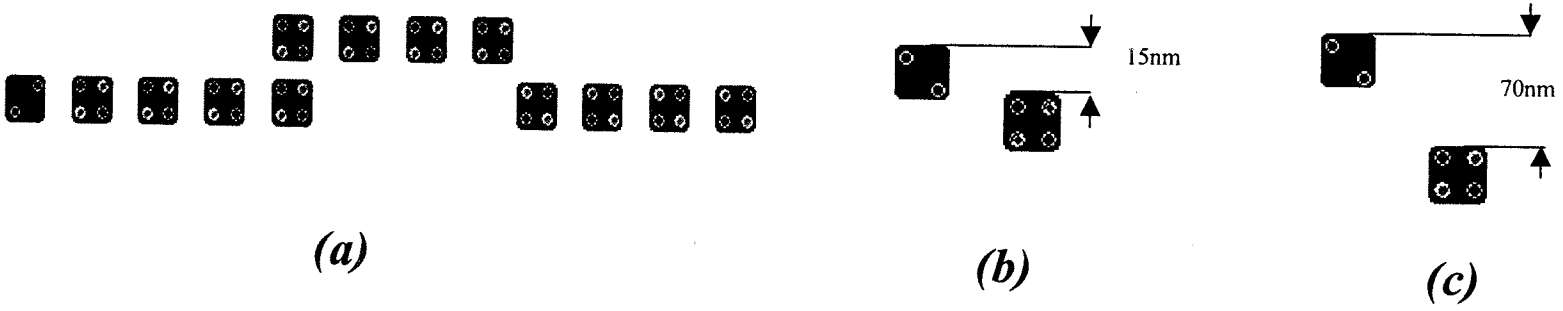

Figure 11. Simpler functioning designs for NOT Gate

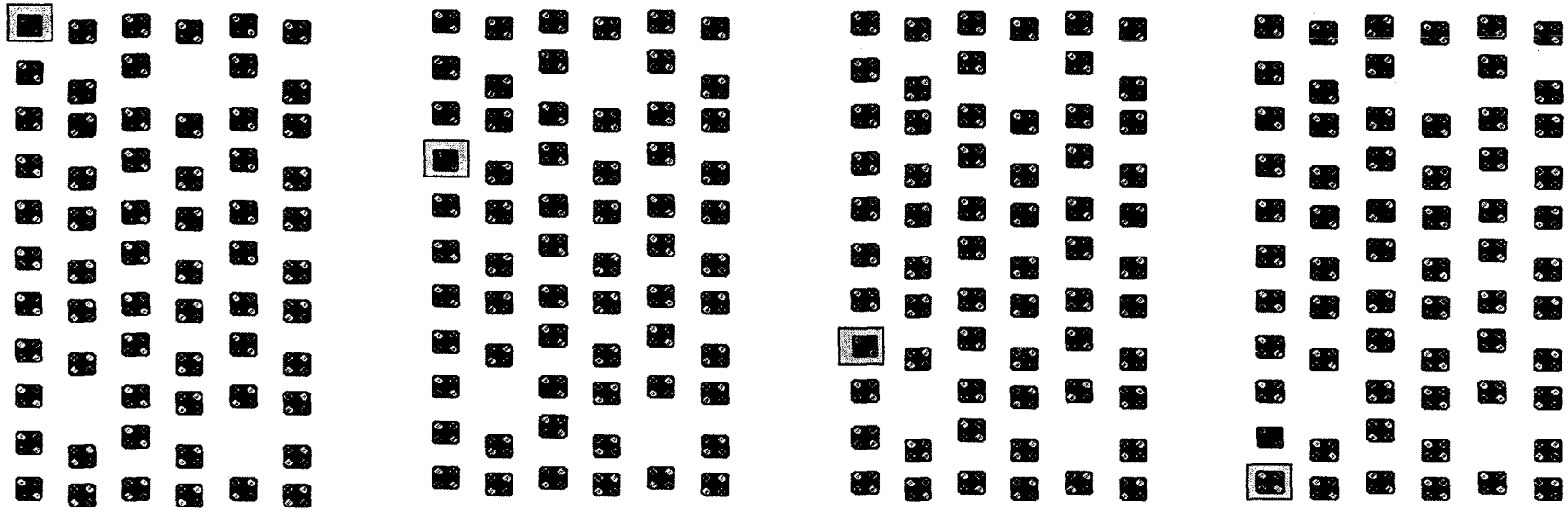

Figure 15. A Block NOT Gate with irregular and defective assembly

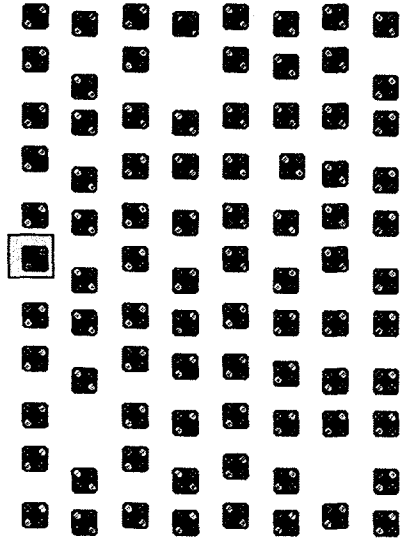

Figure 16. A non-functioning design for Block NOT Gate

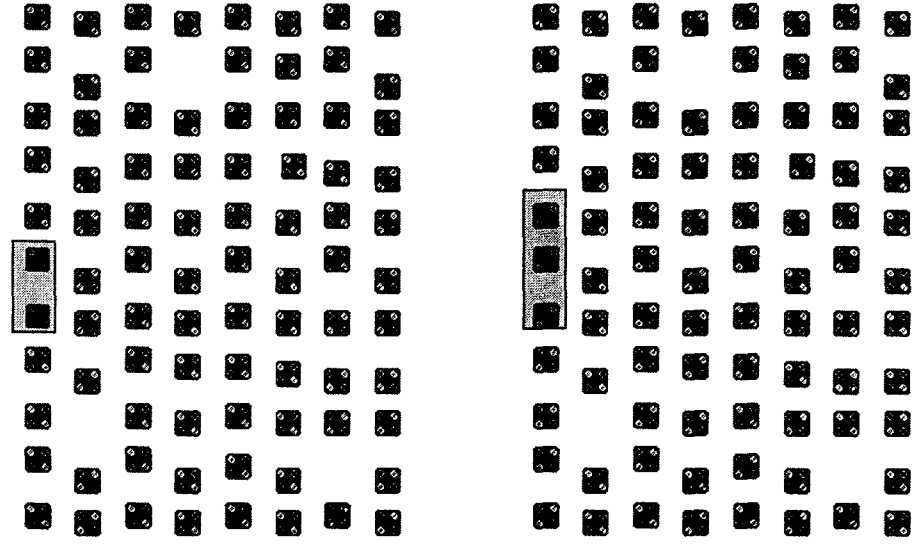

Figure 17. The array of Fig. 16 can properly function as a Block NOT Gate with multiple input cells